

APPENDIX I

A fixed logic zero signal is coupled at node 802 to an input of a shift register comprising flip-flops 816, 818, 820, and 822. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 804. A transmit clock signal is provided to a clock input of the shift register at node 806. Nodes 808, 810, 812, and 814 are coupled to parallel load data inputs of flip-flops 816, 818, 820, and 822, respectively. A serial data output of the shift register at the output of flip-flop 822 is coupled to an input of multiplexer 826 at node 824.